IN THE CLAIMS

1. A ternary content addressable memory (TCAM) device comprising:

A plurality of TCAM cells for storing data, each TCAM cell having two memory cells and a comparison circuit for comparing data stored in the memory cells with data input on a search line pair connected to the comparison circuit, wherein the comparison circuit comprises first, second, third, and forth NMOS transistors, the first and second NMOS transistors having their drains connected to a match line, their gates connected to the memory cells and their source connected to drains of the third and forth NMOS transistors, and the third and forth NMOS transistors having their gates connected to the search line pair and their source connected to ground.

2. The TCAM device according to claim 1, wherein the comparison circuit discharges the match line upon a mismatch between data stored in the memory cells and data input on the search line pair connected to the comparison circuit.

3. The TCAM device according to claim 1, further including a precharge circuit connected to the search line pair for discharging each line of the search line pair to ground upon determination that at least one of the memory cells connected thereto are defective.

4. The TCAM device according to claim 3, wherein the precharge circuit comprises two NMOS transistors, each having its gate connected to a power supply node, its source connected to ground and its drain connected to a corresponding one of the search line pair.

5. The TCAM device according to claim 4, wherein the two NMOS transistors of the precharge circuit are sized to present a low level at the search line pair when no signal is present at the search line pair and to present the same level as a signal asserted at the search line pair.

6. The TCAM device according to claim 3, further including a repair signal generator for generating signals indicating which of the memory cells are defective.

7. The TCAM device according to claim 6, further including redundant TCAM cells and a switching circuit for switching at least a plurality of connections of TCAM cells determined to be defective to corresponding connections of the redundant TCAM cells.

8. The TCAM device according to claim 7, wherein the redundant TCAM cells form at least one column of TCAM cells.

9. The TCAM device according to claim 7, wherein the switching circuit outputs signals for switching connections of a column of TCAM cells having defective cells with corresponding connections of a column of redundant TCAM cells.

10. The TCAM device according to claim 1, wherein the memory cells are SRAM cells.

11. The TCAM device according to claim 1, wherein the memory cells are DRAM cells.

12. A ternary content addressable memory (TCAM) device comprising:

A plurality of TCAM cells for storing data, each TCAM cell having two memory cells and a comparison circuit for comparing between data stored in the memory cells and data input on a search line pair connected to the comparison circuit;

a repair signal generator for generating signals indicating which of the MEMORY cells are defective; and

a precharge circuit connected to the repair signal generator and the search line pair for discharging each of the search line pair to ground upon receipt of signal from the repair signal generator indicating that the memory cells connected thereto are defective.

13. The TCAM device according to claim 12, wherein the comparison circuit comprises a first plurality of MOS transistors connected between a match line and a second plurality of MOS transistors, the second plurality of MOS transistors being connected to ground, wherein the first plurality of MOS transistors are gated by signals from the memory cells connected thereto and the second plurality of transistors are gated by signals from a search line pair.

14. The TCAM device according to claim 12, wherein the first and second plurality of MOS transistors are N type and are

configured to connect the match line to ground upon a mismatch of the data in the corresponding memory cells with the data present at the corresponding search line pair.

15. The TCAM device according to claim 12, wherein the precharge circuit comprises a plurality of MOS transistors having their gates commonly connected to the signal line from the repair signal generator, the plurality of MOS transistors including a pair of transistors for connecting the search line pair to ground and an equalizing transistor for equalizing the search line pair upon receipt of an activating signal at the signal line from the repair signal generator.

16. The TCAM device according to claim 12, further including redundant TCAM cells and a switching circuit for switching at least a plurality of connections of TCAM cells determined to be defective to the redundant TCAM cells.

17. The TCAM device according to claim 16, wherein the switching circuit outputs signals for switching connections of a column of TCAM cells having defective cells with corresponding connections of a column of redundant TCAM cells.

18. The TCAM device according to claim 12, wherein the memory cells are SRAM cells.

19. The TCAM device according to claim 12, wherein the memory cells are DRAM cells.

20. A ternary content addressable memory (TCAM) device comprising:

A plurality of TCAM cells for storing data, each TCAM cell having two memory cells and a comparison circuit for comparing between data stored in the memory cells and data input on a search line pair connected to the comparison circuit, wherein the comparison circuit comprises a first plurality of MOS transistors connected between a match line and a second plurality of MOS transistors, the second plurality of MOS transistors being connected to ground, wherein the first plurality of MOS transistors are gated by signals from the memory cells connected thereto and the second plurality of transistors are gated by signals from a search line pair.

21. The TCAM device according to claim 20, wherein the first and second plurality of MOS transistors are N type and are configured to connect the match line to ground upon a mismatch

of the data in the corresponding memory cells with the data present at the corresponding search line pair.

22. The TCAM device according to claim 20, further including a main search line driver for driving data signals to a plurality of search line pairs and at least one redundant search line driver for replacing the main search line driver upon determination that at least one of the memory cells connected to a corresponding search line pair are defective.

23. The TCAM device according to claim 20, further including a repair signal generator for generating signals indicating which of the memory cells are defective.

24. The TCAM device according to claim 23, further including redundant TCAM cells and a switching circuit for switching at least a plurality of connections of TCAM cells determined to be defective to the redundant TCAM cells.

25. The TCAM device according to claim 24, wherein the switching circuit outputs signals for switching connections of a column of TCAM cells having defective cells with corresponding connections of a column of redundant TCAM cells.

26. The TCAM device according to claim 20, further including a precharge circuit connected to the search line pair for discharging each line of the search line pair to ground upon determination that at least one of the memory cells connected thereto are defective.

27. The TCAM device according to claim 20, further including a memory controller for outputting control signals for controlling operations of the TCAM.

28. The TCAM device according to claim 20, wherein the memory cells are SRAM cells.

29. The TCAM device according to claim 20, wherein the many cells are DRAM cells.

30. A method of operating a ternary content addressable memory (TCAM) device comprising:

comparing data stored in memory cells of the TCAM with data input on a search line pair connected to a comparison circuit, wherein the comparison circuit comprises a first plurality of MOS transistors connected

between a match line and a second plurality of MOS transistors, the second plurality of MOS transistors being connected to ground, wherein the first plurality of MOS transistors are gated by signals from the memory cells connected thereto and the second plurality of transistors are gated by signals from a search line pair.

31. The method according to claim 30, further including switching at least a plurality of connections of TCAM cells determined to be defective to redundant TCAM cells.

32. The method according to claim 31, where the plurality of connections of TCAM cells corresponds to a column of redundant TCAM cells.

33. The method according to claim 30, further including discharging to ground each line of the search line pair upon determination that memory cells connected thereto are defective.